## REMARKS

Applicants have amended claims 1, 5 and 6.

Applicants have amended the specification to over come the objection to the specification that included a typographical error.

Claims 1, 5 and 6 have been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,537,877 (Ishida). Applicants respectfully traverse this rejection.

Claim 1 as amended states that some but not all of the memory transistors are connected with corresponding bit lines by corresponding metal plugs of the one of the insulating layers. This means that the rest of the memory transistors are not connected with any bit lines because no metal plugs are formed at corresponding portions of the one of the insulating layers. This amendment finds support, for example, at page 5, lines 12-19, of the specification and FIGS. 3 and 4 of the application. In the claimed memory device, the connection pattern between the memory transistors and the bit lines is permanent and cannot be changed because there is no way to add or delete the metal plugs once the claimed memory device is manufactured. In other words, the claimed memory device provides a read only memory (ROM). See, for example, page 1, lines 7-9, of the specification.

The Examiner contends that Ishida's static random access memory (SRAM) shown in FIG. 1 of Ishida teaches the claimed memory device. Applicants respectfully disagree. Ishida's SRAM is composed of a plurality of flip-flop circuits each having four memory transistors. In order to operate as a rewritable memory, i.e., SRAM, each of the four transistors of Ishida's flip-flop circuit must be connected to a corresponding bit line. See, for example, column 15, lines 3-27 and FIG. 1 of Ishida. Ishida does not disclose the claimed permanent connection between some but not all of the memory transistors and the bit lines, and especially does not disclose that some memory transistors are not connected with any bit line. All of the memory transistors of Ishida are connected to corresponding bit lines, contrary to the claim language.

Claims 5 and 6 recite ROM memory device structures substantially similar to that of claim 1, which are not disclosed by Ishida. The rejection of claims 1, 5 and 6 under 35 USC

102(b) Ishida should be withdrawn because Ishida does not teach or suggest the claimed permanent connection between the memory transistors and the bit lines.

Claims 1-4 have been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 5,990,507 (Mochizuki). Applicants respectfully traverse this rejection.

The Examiner contends that Mochizuki's ferroelectric random access memory (FRAM) shown in FIG. 2 of Mochizuki corresponds to the memory device of claim 1. However, a RAM, whether it is SRAM, DRAM or FRAM, must have all of its memory transistors connected to corresponding bit lines, as explained above. Such a connection is shown in FIG. 2 of Mochizuki.

The rejection of claims 1-4 under 35 USC 102(b) on Mochizuki should be withdrawn because Mochizuki does not teach or suggest the claim limitation that some memory transistors are not connected with any bit line.

The remaining rejection relies on Mochizuki and thus should be withdrawn as well because Mochizuki does not provide the teachings for which it is cited.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **492322014400**.

Respectfully submitted,

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